**FPGA Engineer**

*Task*

**Counter implementation based on FPGA**

Please complete the following task using structural and functional approaches. Code language is VHDL or Verilog (Xilinx FPGA).

Please study Counter/Delay section in the SLG46620 Datasheet, which you can find at Dialog Semiconductor website (<https://www.dialog-semiconductor.com>). Please design the Counter macrocell using FPGA. Functionality and characteristics should be the same as those of the Counter macrocell of the SLG46620 IC. Please create a logical circuit and timing diagrams for the counter operation.